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EXAMINER	
TRAN, CON P	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,983	BIZJAK, KARL L.	
	Examiner	Art Unit	
	Con P. Tran	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-82* is/are pending in the application.

4a) Of the above claim(s) *27-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 44-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 27-33, and 34-43 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on July 08, 2005.

2. Applicant's election with traverse of the restriction requirement in the reply filed on July 08, 2005 is acknowledged.

The traversal of claims 72-73 is on the ground that these claims are not limited to frequency control. This is found persuasive. Accordingly, claims 72-73 are rejoined.

The traversal is on the ground that one example of an embodiment associated with claims 34-43 a signal processor may be used for amplitude adjustment. This is not found persuasive because the claims are drawn to frequency control, i.e., a filter to vary or maintain frequency response.

The traversal is on the ground that the preamble of claims 27-33 have been amended with the term "signal processor". This is not found persuasive because the body of the claim is a self-contained description of an equalizer that could stand alone, with or without the preamble.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

3. Figures 1A-1E, and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6, 8-19, and 44-46** are rejected under 35 U.S.C. 102(b) as being anticipated by Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani").

Regarding **claim 1**, Kitani teaches a compander (see Figs. 1, 4, 5, and respective portions of the specification), comprising:

an input signal (10, Figs. 1, 4, 5)

gain calculate logic (including rectifier 13, comparator 15, second volume 18; Figs. 1, 4, 5) responsive to the input signal (10) for calculating a gain calculate signal (out put of 15; see col. 1, lines 38-58; col. 6, lines 8-12);

synchronizer logic (including up/down counter 16, programmable counter 19, first volume 11; Figs. 1, 4, 5, 6) responsive to the input signal (10) and the gain calculate signal (out put of 15) for synchronizing the input signal and the gain calculate signal to provide an output signal (col. 3, lines 29-40; col. 6, lines 18-49; co. 8, lines 11-19);

Regarding **claim 2**, Kitani teaches wherein the synchronizer logic includes a gain cell (11c, 11b, Figs. 5, 10; col. 8, lines 38-43).

Regarding **claim 3**, Kitani teaches wherein the synchronizer logic further includes a synchronizer block (programmable counter 19 and up/down counter 16; Figs. 4, 5).

Regarding **claim 4**, Kitani teaches wherein the synchronizer block (programmable counter 19 and up/down counter 16; Figs. 4, 5) provides a gain signal (11c, 11b, Figs. 5, 10) and a delayed signal to the gain cell (col. 16, lines 13-26; lines 47-53), and the gain cell output is the output signal (col. 3, lines 8-13; col. 8, lines 38-43).

Regarding **claims 5 and 6**, Kitani teaches the compander of claim 1 wherein the gain calculate logic includes detection logic (comparator 16, Figs. 1, 4, 5) for detecting a predetermined condition of the input signal including zero crossing (alternate switching high level, low level), and wherein the gain calculate signal is generated only after the predetermined condition of the input signal occurs (down counting, up counting; col. 7, lines 43-60).

Claims 8-9, 11, and 13-15 are also met, i.e., monitoring input logic (col. 3, 44-52), power estimator logic (low pass filter 14, Figs. 4, 5), alternate switching high level, low level; down counting, up counting, peak (col. 7, lines 43-60), average, DC voltage, i.e., RMS, (col. 12, lines 42-67).

Claims 10, 12, and 16-19 are met in view of above discussion of **Claims 8-9, 11, and 13-15,** reset, i.e., ON/OFF operation of the switch (74a, col. 14, lines 1-9), also please see col. 16, lines 12-55, Figs. 32, 33(A)-33(K).

Regarding **claims 44-46,** Kitani teaches a compander having an input comprising at least one power estimator signal (low pass filter 14, Figs. 4, 5), first signal processing stage for processing the at least one power estimator signal (output of LPF 14; col. 7, lines 43-60); wherein the processing is demodulating (col. 11, lines 1-10), wherein processing is filtering (low pass filtering).

6. **Claims 50-59, and 72-82** are rejected under 35 U.S.C. 102(b) as being anticipated by Lemson U.S. Patent 5,457,811.

Regarding **claim 50,** Lemson teaches a compander (see Figs. 6, 6a, and respective portions of the specification) having:

a first input (61a, Fig. 6) comprising at least one local power estimator signal (output of 56, Fig. 6; col. 26, lines 42-64; col. 28, lines 5-19),

a second input (61b, Fig. 6) comprising at least one external power estimator signal (energy determiner, see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33),

a first signal processor (combiner 60, Fig. 7) for processing the first input (61a, Fig. 6) and the second input (61b, Fig. 6) to produce a first output (61b, Fig. 6; col. 26, lines 42-64).

Claims 51-52 are met since processor (combiner 60, Fig. 7) selecting and combining the two inputs.

Regarding **claim 53,** Lemson teaches wherein the processing includes scaling at least one of the first and second inputs (weighting, col. 28, lines 5-19).

Regarding **claim 54,** Lemson teaches the compander of claim 50 wherein the second input (61b, Fig. 6) comprises a plurality of external power estimator signals (Fig. 6a) and further including a second signal processor (AC processor 58, including threshold detector, clock, Fig. 6a) for processing the plurality of external power estimator signals to produce a single output signal (61b) to the first signal processor (60; col. 26, 55-65; col. 29, 27-33).

Regarding **claims 55-56,** Lemson teaches wherein the processing performed by the second signal processor includes combining (for selection, see Fig. 6a), selecting at least some of the plurality of external power estimator signals (see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33).

Regarding **claim 57,** Lemson teaches wherein the processing performed by the second signal processor includes scaling at least one of the plurality of external power estimator signals (weighting, col. 28, lines 5-19).

Regarding **claim 58,** Lemson teaches wherein the processing performed by the second signal processor includes being capable of demodulating at least one of the plurality of external power estimator signals (col. 5, lines 42-53).

Regarding **claim 59,** Lemson teaches wherein the processing performed by the second signal processor includes filtering at least one of the plurality of external power estimator signals (BPF, Fig. 6a).

Regarding **claims 72-73,** these claims merely reflect the method to the apparatus claim of claims 50 and 54 and are therefore rejected for the same reasons.

Regarding **claim 74,** Lemson teaches a compander (see Figs. 6, 6a, and respective portions of the specification) having:

a first plurality of external power estimator signals (see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33);

processing stage for combining at least some of the first plurality of power estimator signals and for generating at least one output signal (for selection, see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33).

Regarding **claim 75,** Lemson teaches a compander (see Figs. 2, 13, and respective portions of the specification; col. 16, lines 22-50; col. 25, lines 23-63) having: a first external power estimator signal, a second external power estimator signal (e.g., 3 and 4; col. 25, lines 45-55), a first signal processor (microprocessor 100, Fig. 13) for processing the first and second power estimator signals to produce a first output

wherein processing includes at least one of a group comprising scaling, combining and selecting the first and second power estimator signals (combining and selecting to form look-up table; col. 25, lines 23-42).

Regarding **claim 76,** Lemson teaches wherein the processing includes demodulating at least one of the external power estimator signals (col. 5, lines 42-53).

Regarding **claim 77,** Lemson teaches wherein the processing includes scaling at least one of the external power estimator signals (e.g., via attenuator; col. 5, lines 42-53).

Regarding **claim 78,** Lemson teaches wherein the processing includes filtering at least one of the external power estimator signals (BPF, Fig. 6a; col. 13, lines 58-64).

Regarding **claim 79,** Lemson teaches further including a second signal processor for processing the first output (including controller 42, modulator 22, microprocessor 100, Fig. 13; col. 25, lines 23-42).

Regarding **claim 80,** Lemson teaches wherein the second signal processor modulates the first output (by modulator 22, Fig. 13).

Regarding **claim 81,** Lemson teaches wherein the second signal processor scales the first output (e.g., via attenuator; col. 5, lines 42-53; col. 12, lines 39-46).

Regarding **claim 82,** Lemson teaches wherein the second signal processor filters the first output (BPF, Fig. 6a; col. 13, lines 58-64).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Thomas U.S. Patent 4,947,133 (cited by Applicant).

Regarding **claim 7,** Kitani teaches the compander of claim 6. However, Kitani does not explicitly disclose wherein the predetermined condition of the input signal further includes a failure to have a zero crossing within a predetermined period.

Thomas discloses a failure to have a zero crossing within a predetermined period in col. 6, line 63 – col. 7, line 8 (i.e., exceed delay).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a predetermine condition of Thomas teaching with the predetermine condition of Kitani such that including a failure to have a zero crossing within a predetermined period for purpose of having a control transfer function that may be provided by a digital low-pass filter clocked at zero crossings of the input signal, as suggested by Thomas in column 1, lines 57-59.

9. **Claims 20-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Germer U.S. Patent 4,628,526 (cited by Applicant)

Regarding **claim 20,** Kitani teaches the compander of claim 8. Kitani further teaches wherein the power estimator logic includes initial power estimator logic for determining an initial power estimate (output of LPF 14, Figs. 4, col. 7, lines 43-60), and variable attack and release logic responsive to the initial power estimate (col. 7, lines 61 – col. 8, line 32; Figs. 9A-9C). However, Kitani does not explicitly disclose wherein an initial power estimate for determining a rate of change for the gain calculate signal. Germer discloses matching sound output in which envelope curve detectors (15) and (16) respectively present at the inputs a and b of the comparison circuit (17) are

respectively connected to differentiators (19, 20) which responses to changes in envelope curve signals (Figs. 1, 2; col. 6, lines 22-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate differentiators of Germer teaching with compander of Kitani to have an initial power estimate for determining a rate of change for the gain calculate signal as claimed for purpose of having an automatic loudspeaker volume control that is independent of influences of the characteristic of the loudspeaker location, as suggested by Germer in column 2, lines 3-5.

Regarding **claims 21-23,** Kitani as modified teaches a plurality of variable attack and release modules (see Figs 9A-9C), wherein the initial power estimator logic provides at least first and second power estimator signals, and wherein the variable attack and release logic compares the first power estimator signal with the second power estimator signal (attack time, recovery time become shorter); variable attack and release logic responsive to the initial power estimate (col. 7, lines 61 – col. 8, line 32); .

Regarding **claims 25-26,** Kitani as modified discloses using plurality of resistors, capacitor for low pass filtering. It would have been obvious to one of ordinary skill in the art to add a preliminary power estimator which receives as an additional input the output of the variable attack and release logic for purpose of providing both the compressor characteristic and the expander characteristic, as suggested by Kitani in column 3, lines 23-24.

10. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Germer U.S. Patent 4,628,526 (cited by Applicant), and further in view of Orban U.S. Patent 5,444,788.

Regarding **claim 24,** Kitani in view of Germer teaches the compander of claim 20. Kitani further teaches wherein the initial power estimator logic provides at least one power estimator signal to the variable attack and release logic (col. 7, lines 61 – col. 8, line 32). However, Kitani in view of Germer does not explicitly disclose wherein the output of the variable attack and release logic is fed back to provide a second input to the variable attack and release logic.

Orban discloses an audio compressor having a feedback compressor (including VCA 120, rectifier 150, timing circuit 170, and summation means 205, see drawing) operated as a pilot device coupled between RELEASE TIME control device (210) and the gain of VCA (120; see col. 3, lines 35-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a feedback compressor of Orban teaching with the compander of Kitani, Germer in combination such that output of the variable attack and release logic is fed back as claimed for purpose of producing a "soft-knee" characteristic, as suggested by Orban in column 4, lines 45-48.

11. **Claims 47-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitani et al. U.S. Patent 4,709,296 (hereinafter, "Kitani") in view of Glaberson U.S. Patent 4,376,916.

Regarding **claim 47,** Kitani teaches the compander of claim 44. However, Kitani does not explicitly disclose wherein at least one power estimator signal is a plurality of power estimator signals. Glaberson discloses improved signal compression and expansion system in which one power estimator (output of sum 30, Fig. 1) is sum of a plurality of power estimator signals (36, 42, 48; col. 4, lines 39-44; col. 6, lines 46-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporate a plurality of power estimator signals of Glaberson teaching with the compander of Kitani so that the at least one power estimate signal is a plurality of power estimator signals for purpose of removal minor ripples not associated with perceptible changes in the information signal, as suggested by Glaberson in column 6, lines 42-45.

Claim 48 is met since signals are combined at sum 30, Fig. 1.

Regarding **claim 49,** Kitani in view of Glaberson teaches wherein the processing is selecting a preferred one of the plurality of power estimator signals (e.g., 0 dB; see Glaberson, Fig. 4, col. 13, lines 18-31) .

12. **Claims 60-71** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lemson U.S. Patent 5,457,811.

Regarding **claim 60,** Lemson teaches the compander of claim 50. However, Lemson does not explicitly disclose wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal as claimed.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, having a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal as claimed for purpose of increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 61,** Lemson, as modified, further teaches wherein the third signal processor comprises a plurality of signal processors, each of which produces an exported power estimator signal signals (see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33).

Regarding **claims 62-63,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes combining (for selection, see Fig. 6a), selecting at least some of the plurality of local estimator signals (see 58, Figs. 6, 6a; col. 26, lines 42-64; col. 29, 27-33).

Regarding **claim 64,** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes scaling at least one of the plurality of local power estimator signals (weighting, col. 28, lines 5-19).

Regarding **claim 65,** Lemson, as modified, teaches wherein the processing performed by the third signal processor includes modulating at least one of the plurality of local power estimator signals (see col. 4, line 64 – col. 5, line 7).

Regarding **claim 66,** Lemson, as modified, teaches wherein the processing performed by the third signal processor includes filtering at least one of the plurality of local power estimator signals (BPF, Fig. 6a).

Regarding **claim 67,** Lemson, as modified, teaches further including a second signal processor for processing the second input signal (AC processor 58, including

threshold detector, clock, Fig. 6a) for processing the plurality of external power estimator signals to produce a single output signal (61b) to the first signal processor (60; col. 26, 55-65; col. 29, 27-33) and a third signal processor (DC processor 56, Fig. 6) for processing the first input signal to produce an exported power estimator signal (col. 26, lines 42-64; col. 28, lines 5-19).

Regarding **claim 68,** Lemson, as modified, teaches wherein the second input comprises a plurality of local power estimator signals (output energy determiners, Fig. 6a) and the second signal processor processes at least one of the local power estimator signals to produce a single output signal to the first signal processor (AC processor 58, including threshold detector, clock, Fig. 6a).

Regarding **claim 69,** Lemson, as modified, teaches the compander of claim 68. However, Lemson does not explicitly disclose wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal as claimed.

Nevertheless, it is known in the art to duplicate parts for multiple effects. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

In this regard, having a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal as claimed for purpose of

increasing capacity of processing signal would have been considered obvious for one of ordinary skill in the art.

Regarding **claim 70** Lemson, as modified, teaches wherein the processing performed by the second signal processor includes demodulating the second input signal (col. 5, lines 42-53).

Regarding **claim 71,** Lemson, as modified, teaches the processing performed by the second and third signal processor including modulating the first input signal (col. 4, line 64 – col. 5, line 7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Con P. Tran whose telephone number is (571) 272-7532. The examiner can normally be reached on M - F (8:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Vivian C. Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cpt CPJ
October 24, 2005

XU MEI
PRIMARY EXAMINER